AC-4049

B.Tech. (3rd sem.) Examination, 2013
Computer Sci. & Engg.
Subject: Digital Logic & Design.
Maximum Marks: 60

Section A

Question (1): choose the correct answer:

Answer (i) (c) Propagation Time
(ii) (a) Rise Time
(iii) (d) XOR gate
(iv) (d) OR gate
(v) (a) OR gates and AND gates only
(vi) (a) Combinational logic circuits
(vii) (a) 10111 0000
(viii) (c) Both (a) & (b)
(ix) (a) is slower
(x) (b) to select 1 out of N input data sources and to transmit it to single channel.

Section - B

Que: (2) :-

Answer (2):- $= (x+y)\,(\bar{x}+z)\cdot(y+z)$

$= (x\cdot\bar{x} + x\cdot z + \bar{x}\cdot y + y\cdot z)(y+z)$

{∵ By Distributive law}

$= x\cdot y\cdot z + \bar{x}\cdot y\cdot y + y\cdot y\cdot z + x\cdot z\cdot z + \bar{x}\cdot y\cdot z + y\cdot z\cdot z$

{∵ $A\cdot\bar{A}=0$, Distributive law.}

$= x\cdot y\cdot z + \bar{x}\cdot y + y\cdot z + x\cdot z + \bar{x}\cdot y\cdot z + y\cdot z$

{∵ $A\cdot A = A$}

$= x\cdot y\cdot z + \bar{x}\cdot y + y\cdot z + \bar{x}\cdot y\cdot z + x\cdot z$

{∵ $A+A=A$}

$= x\cdot y\cdot z + \bar{x}(y+yz) + y\cdot z + x\cdot z$

{∵ By Associative law $(A+AB=A)$}

$= x\cdot y\cdot z + \bar{x}\cdot y + y\cdot z + x\cdot z$ {∵ A. Law.}

$= x\cdot z\,(y+1) + \bar{x}\cdot y + y\cdot z$ {∵ A. Law}

$= x\cdot z + \bar{x}\cdot y + y\cdot z$ {∵ $A+1=1$ Identity law.}

$= x\cdot\bar{x} + x\cdot z + \bar{x}\cdot y + y\cdot z$ {∵ $A\cdot\bar{A}=0$}

$= (x+y)\cdot\bar{x} + (x+y)\cdot z$ {∵ A. Law.}

$= (x+y)\cdot(\bar{x}+z)$ {∵ A. Law}

Que. (3) :-

Ans (3) :- subtract 35 - 45 using 9's complement.

$$\begin{array}{r} 99 \\ -45 \\ \hline 54 \\ +35 \\ \hline \boxed{0}\,89 \end{array}$$

By 9's complement.

No carry

then

$$\begin{array}{r} 99 \\ -89 \\ \hline 10 \end{array}$$

Ans = $-(10) = -10$ Ans

Que. (4)

Ans (4) 16's complement of the F20.3AE

∵ 15's Complement is

$$\begin{array}{r} FFF.FFF \\ -\ F20.3AE \\ \hline 0DF.C51 \\ +\ 1 \end{array}$$

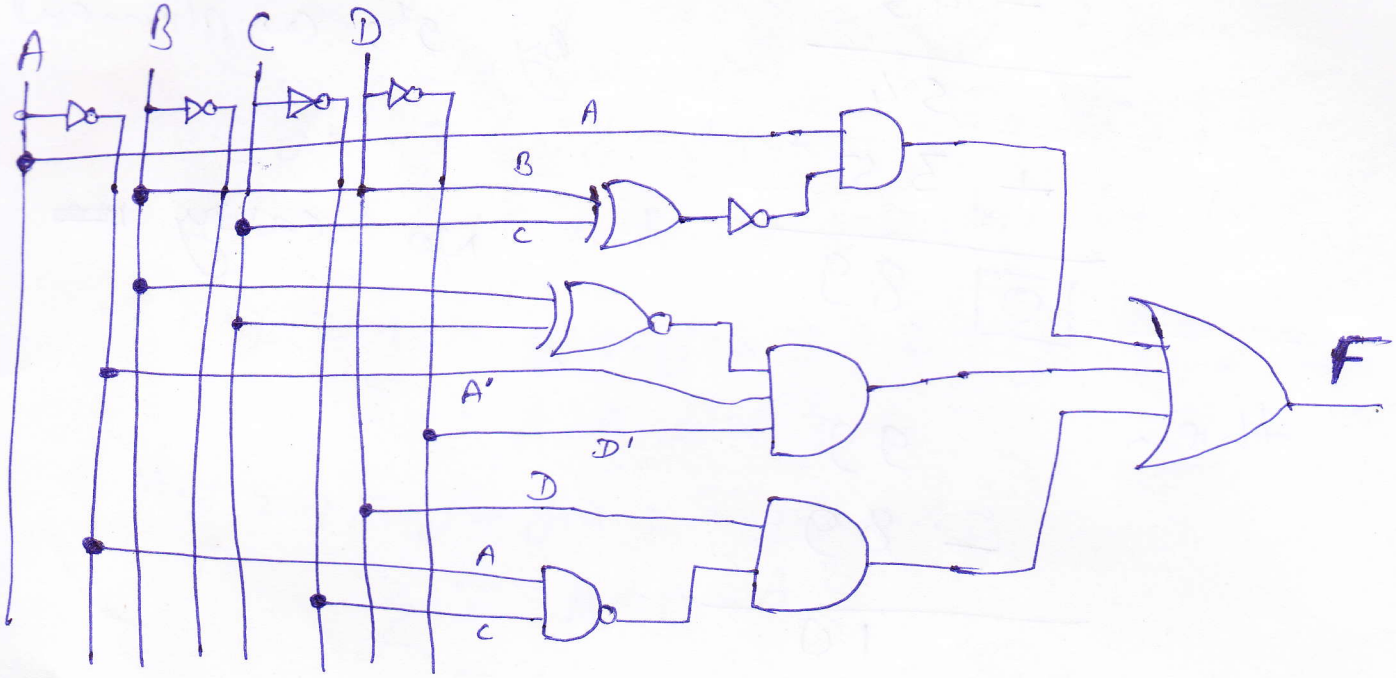
16's Complement

Unit - II

Que (5) :-

Ans (5) :- Draw the circuit diagram.

$$F = A \cdot \overline{(B \oplus C)} + (B \odot C)\,\bar{A}\,\bar{D} + D \cdot (\overline{A \cdot C})$$



Que. (6) :-

Ans :- $F(A, B, C, D) = \sum \pi (4, 5, 6, 7, 8, 12) + d(0, 1, 2, 3, 9, 11, 14)$

AB \ CD	00	01	11	10
00	X (0)	X (1)	X (3)	X (2)
01	0 (4)	0 (5)	0 (7)	0 (6)
11	0 (12)	1 (13)	1 (15)	X (14)
10	0 (8)	X (9)	X (11)	1 (10)

S.O.P. $F = A \cdot D + A \cdot C$ — (1) ~~S.O.P.~~

Que (7):→

Ans (7):→ Tabulation Method.

$\therefore F = \sum m(0,1,2,8,10,11,14,15)$

	(a)		(b)		(c)	
	w x y z		w, x, y, z		w x y z	
0	0 0 0 0	✓	(0,1)	0 0 0 -	(0,2,8,10)	- 0 - 0
1	0 0 0 1	✓	(0,2)	0 0 - 0 ✓	(0,8,2,10)	- 0 - 0
2	0 0 1 0	✓	(0,8)	- 0 0 0 ✓		
8	1 0 0 0	✓	(2,10)	- 0 1 0 ✓	(10,11,14,15)	1 - 1 -
10	1 0 1 0	✓	(8,10)	1 0 - 0 ✓	(10,14,11,15)	1 - 1 -
11	1 0 1 1	✓	(10,11)	1 0 1 - ✓		
14	1 1 1 0	✓	(10,14)	1 - 1 0 ✓		
15	1 1 1 1	✓	11,15	1 - 1 1 ✓		
			14,15	1 1 1 - ✓		

Ans: $w'x'y' + x'z' + wy.$

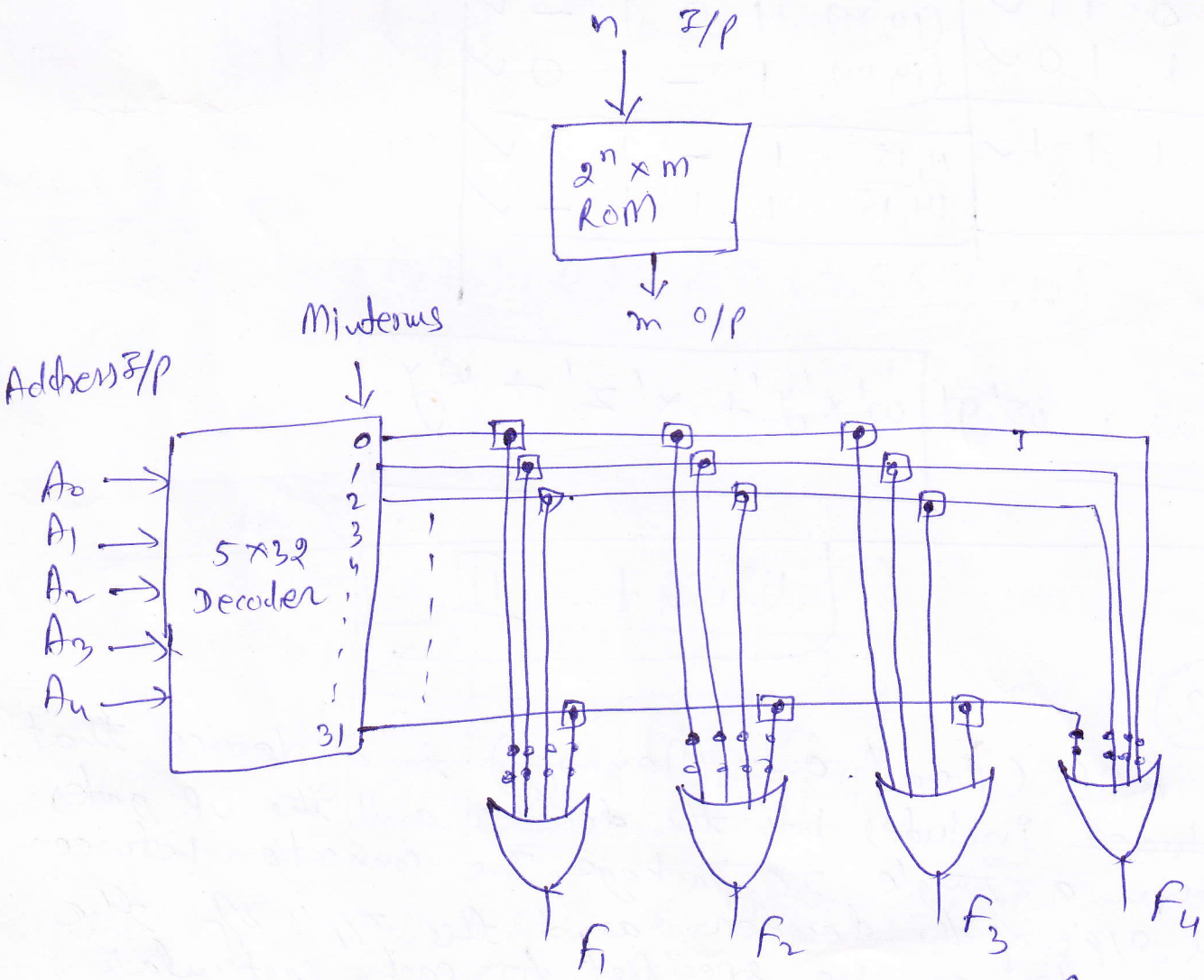
Unit - III

Que (8)

Ans: ROM (Read only Memory) is a device that ~~included~~ includes both the decoder and the OR gates within a single IC package. The connection between the O/P's of the decoder and the I/P's of the OR gates can be specified for each particular

circuit in one IC package and thus eliminate all interconnecting wires.

A ROM is essentially a memory (or storage) device in which a fixed set of binary information is stored. The binary information must first be specified by the user and is then embedded in the unit to form the required interconnection pattern. ROM's come with special internal links that can be fused or broken. The desired interconnection for a particular application requires that certain links be fused to form the required circuit paths. Once a pattern is ~~essential~~ established for a ROM, it remains fixed even when power is turned off and then on again.

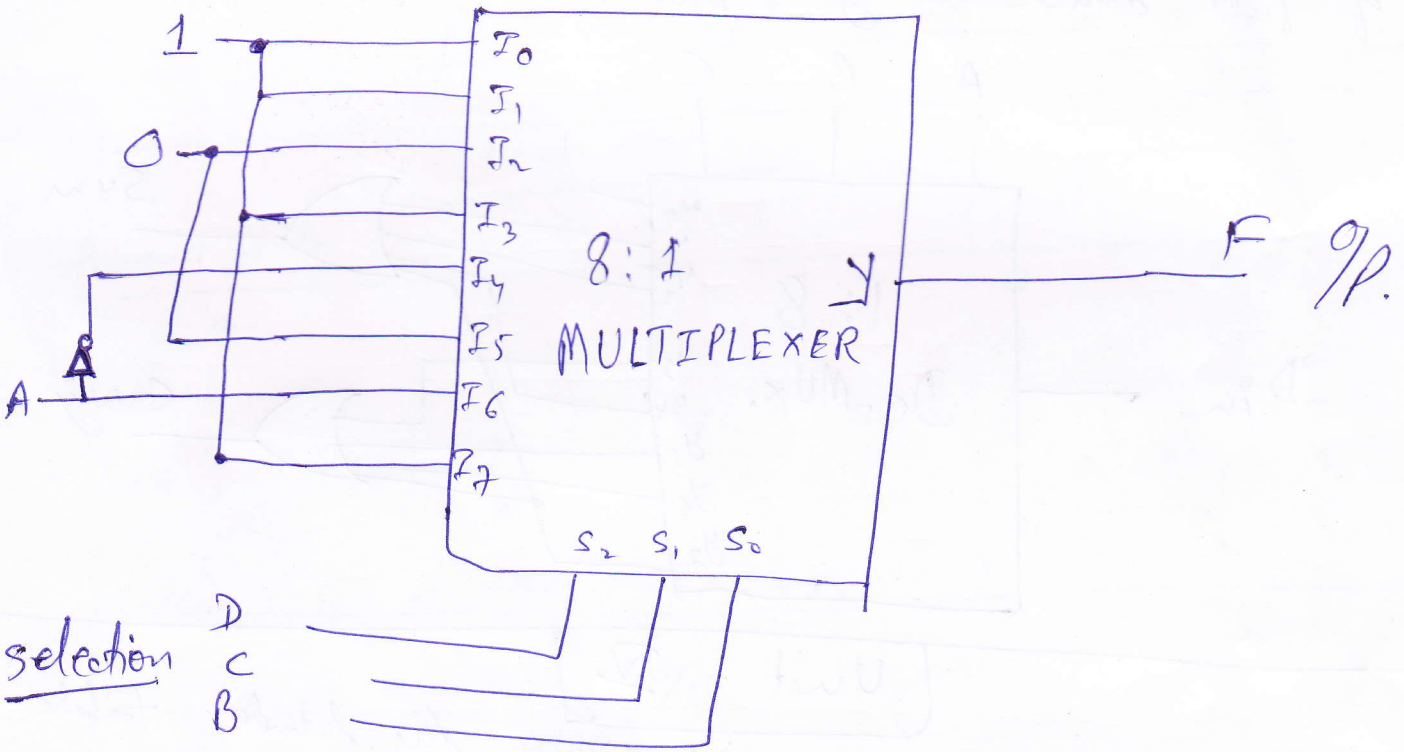


Que (9):-

Ans :- Implement 8:1 multiplexer.

$$F(A,B,C,D) = \Sigma m(0,1,3,4,7,8,9,11,14,15)$$

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	1	1	0	1	A'	0	A	1



Que. (10):-

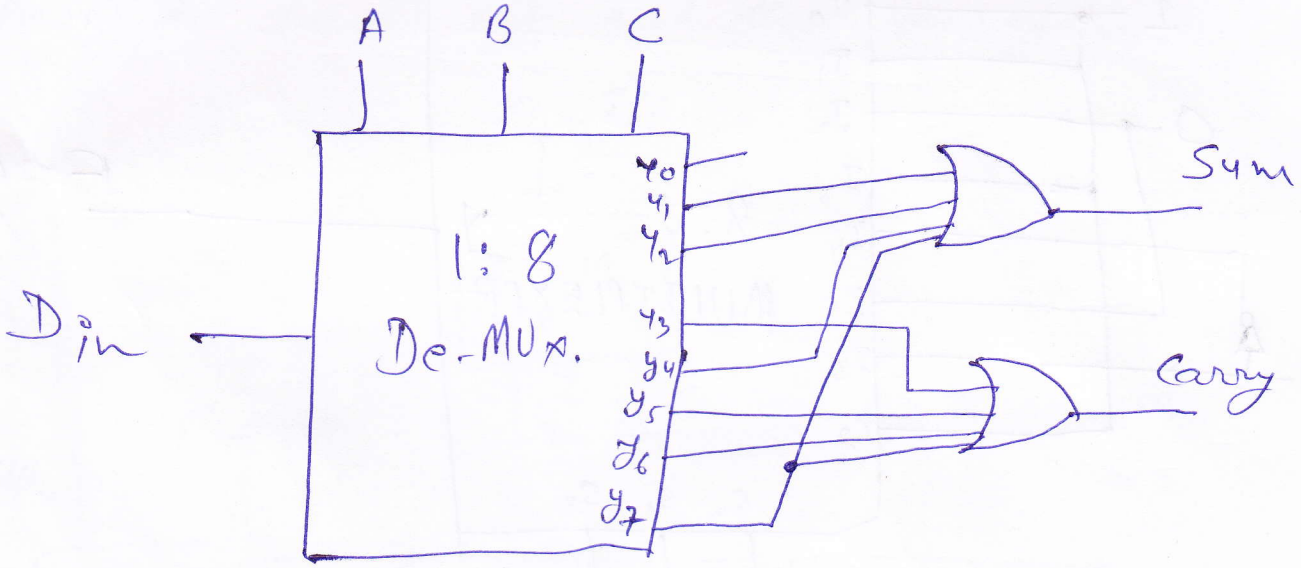
Ans. :- Each o/p of Demultiplexer is a minterm. So we can easily implement the full adder. The canonical form of Sum and carry

$$Sum = \Sigma m(1,2,4,7)$$

Truth Table of full adder:

I/P			O/P	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Demultiplexer gives minterms at the o/p, so we can implement Boolean function for Full Adder by logically ORing required minterms. The implementation of full adder using Demultiplexer is in fig.



Unit - IV

Que (11):- Reducing the State table

Ans:

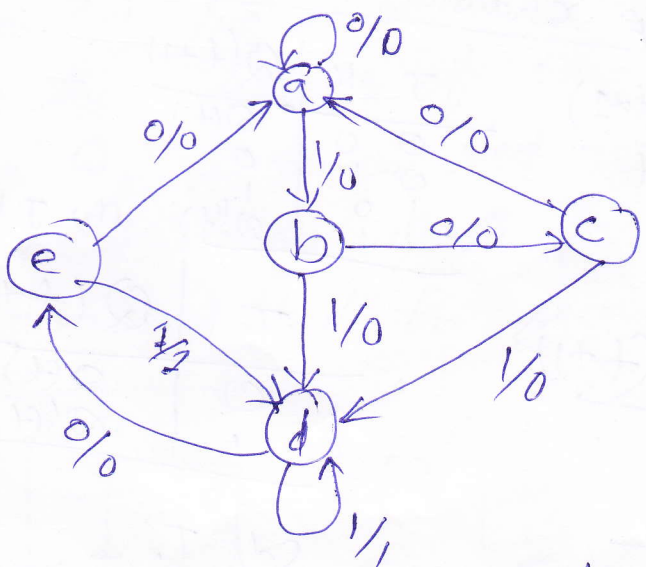
Present state	Next state		O/P.	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1

we look for two present states that go to the same next state and have the same o/p for both I/P combinations. States g and e are two such states; they both go to states a and f and have o/p's of 0 and 1 for $x=0$ and $x=1$, respectively. Therefore, states g and e are equivalent; one can be removed.

Present state f now has next states e and f and o/p 0 and 1 for $x=0$ and $x=1$, respectively. The same next states and o/p appear in the row with present state d. Therefore, states f and d are equivalent; state f can be removed and replaced by d.

Reduced State table

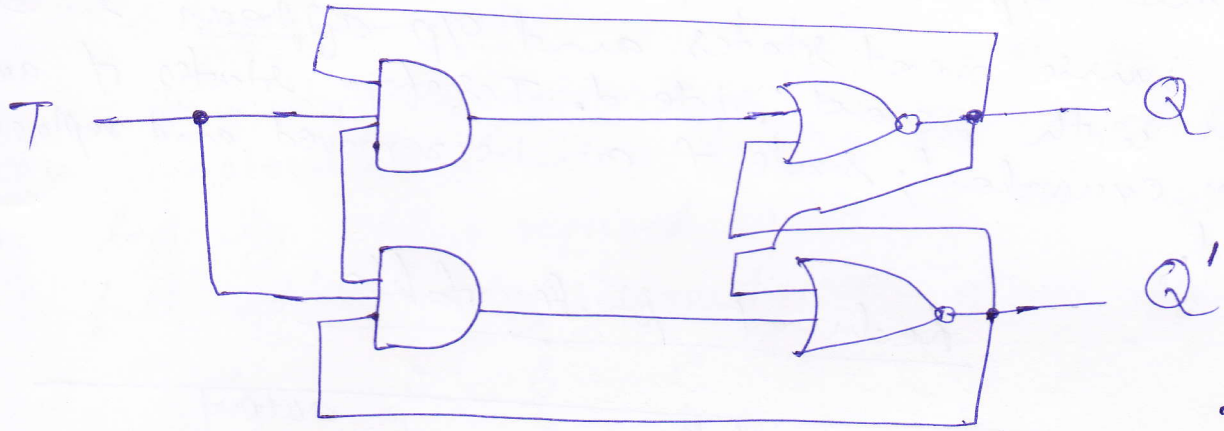
Present state	Next state		output	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

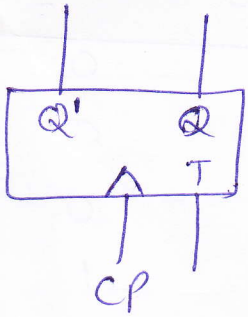


State	a	a	b	c	d	e	d	d	e	d	e	e
I/P	0	1	0	1	0	1	1	0	1	0	0	
O/P	0	0	0	0	0	1	1	0	1	0	0	

Que. (12)

Ans. T- F/F. Logic Diagram.





Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Q \ T	0	1
0		1
1	1	

$Q(t+1) = TQ' + T'Q$

Que (13) ...

Ans :- F/F characteristic Tables

S	R	Q(t+1)
0	0	Qt
0	1	0
1	0	1
1	1	?

(a) RS

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

(b) JK

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

(d) T.

F/f excitation Tables

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

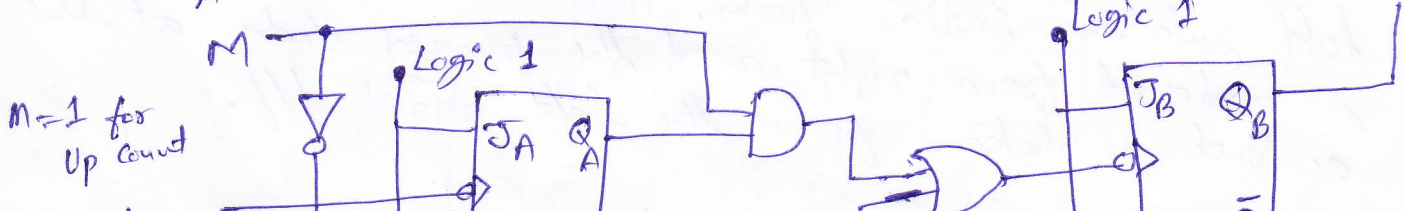
Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Unit - IV

Que. (14):

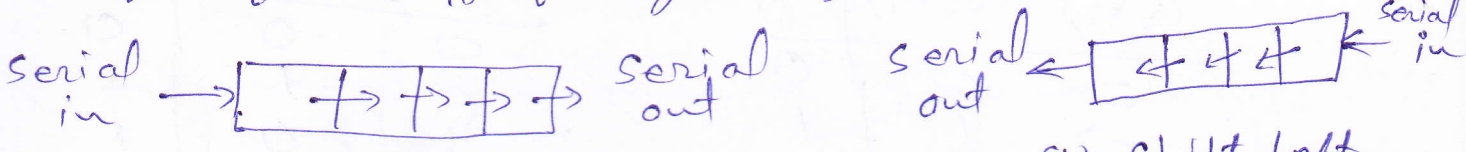
Ans:- 2-bit Ripple Up/Down Counter.

Up-Down counter is a counter which can count both in upward (ascending) and downward (Decending order) directions. It is also called a forward/backward counter or bidirectional counter. So, a control signal or a mode signal M is used to choose the directions of count. When M=1 for upcounting, Q_A is transmitted to clock of second flip-flop and when M=0 for down counting, $\overline{Q}_A$ is transmitted to second f/f.



Ques (15):-

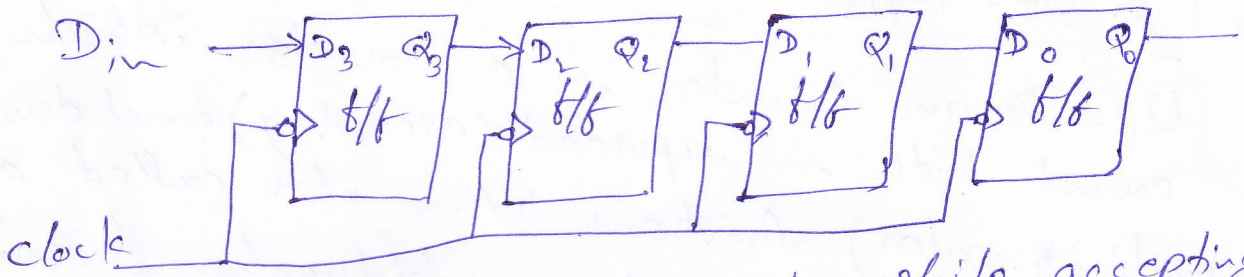
Ans: The serial in serial out shift register accepts the data serially on a single input line. It also produces the stored information on its output in serial form. We can shift the data from left side or right side. Based on the shifting of data, the register is called shift left or shift right register.



(a) Shift Right (b) Shift Left.

Fig: 4-bit serial in serial out shift register.

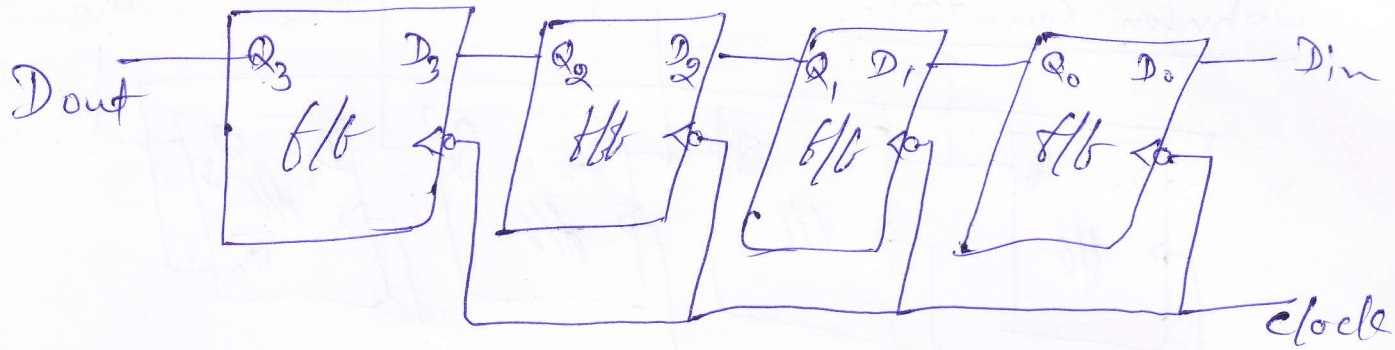
(i) Shift Right Register:-



In this shift register while accepting data serially, the group of bits is shifted towards the right side. Hence the serial data is entered into the left side of register and it leaves from the right side serially.

(ii) Shift Left Register:-

The group of bits is shifted toward the left side in serial form. Hence the serial data is entered from right and the binary data at the output is taken from the left most f/f.



Que. (16) :-

Ans: A shift register counter is basically a shift register with the serial o/p connected back to the serial input to produce special sequences. These devices are classified as counters because they exhibit a special sequence of states. Two of the most common types of shift register counters are the ring counter and the Johnson counter.

Ring Counter :- It is constructed from shift registers of any length n, where n is the number of f/f. D-f/f result in the simplest circuit. The o/p of the first f/f Q_0 is connected to the i/p of second f/f and so on.

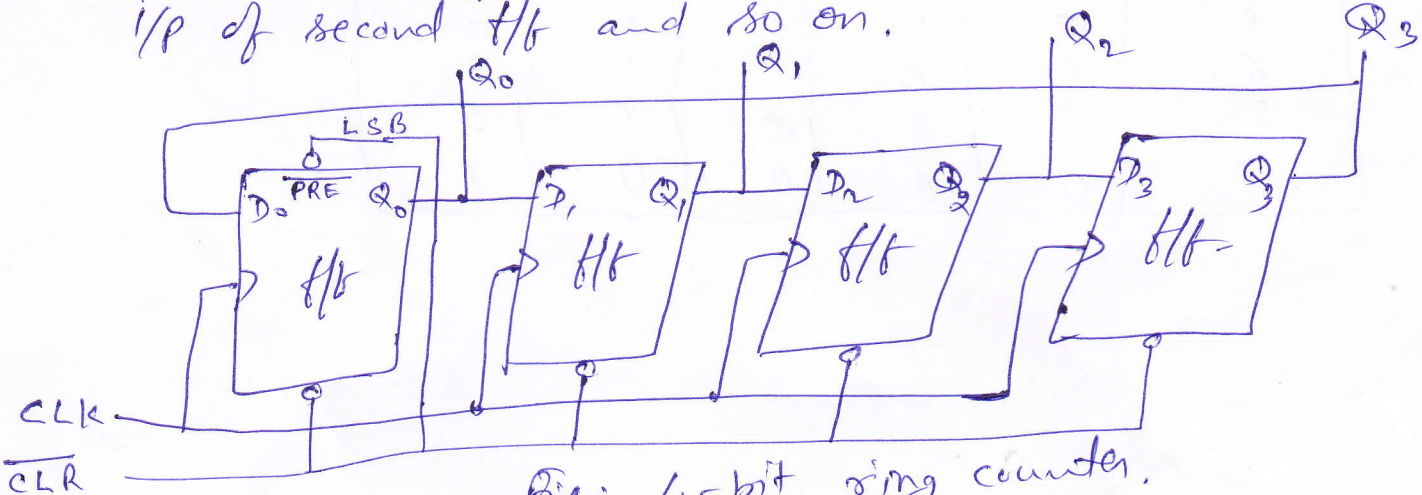
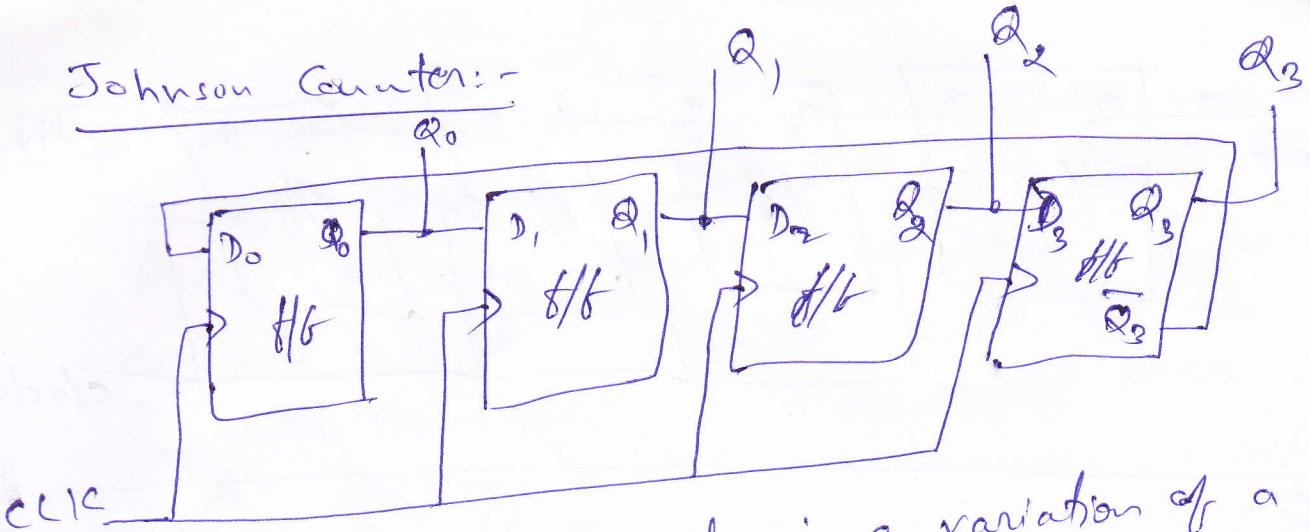


Fig :- 4-bit ring counter.

T.T.

CLK	$\overline{CLR}$	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	1
1	1	0	0	1	0
1	1	0	1	0	0
1	1	1	0	0	0

Johnson Counter:-



The Johnson counter is a variation of a shift register counter. Johnson counters have basic counting cycles of length 2N. where N is the number of f/f. In Johnson counter, the complement of the o/p of the last f/f is connected back to the D-input of the first f/f. This feedback arrangement produces a unique sequence of states.

clock	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$
0	0	0	0	0	1
1	1	0	0	0	1
2	1	1	0	0	1
3	1	1	1	0	1
4	1	1	1	1	0
5	0	1	1	1	0
6	0	0	1	1	0
7	0	0	0	1	0
8	0	0	0	0	1